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Terms used
design$4 same id$1 identif$4 same portion$4 same file$1 same figur$4 same element$1 same generat$4 s

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1 A Hierarchical Test Scheme for System-On-Chip Designs

J. Li, H. Huang, J. Chen, C. Su, C. Wu, C. Cheng, S. Chen, C. Hwang, H. Lin

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(106.56 KB) Publisher Site

Additional Information: full citation, abstract

System-on-chip (SOC) design methodology is becomingthe trend in the IC industry. Integrating multiple sources is essential in SOC design, and differentdesign-for-testability methodologies ar testing different cores. Another issue is test integration.The purpose of this paper is to present scheme for SOC with heterogeneous core test andtest access methods. A hierarchical test mana proposed to generate the control signals for th ...

2 Broadcast protocols to support efficient retrieval from databases by mobile users

Anindya Datta, Debra E. VanderMeer, Aslihan Celik, Vijay Kumar

March 1999 **ACM Transactions on Database Systems (TODS)**, Volume 24 Issue 1

Publisher: ACM Press

Full text available: pdf(638.48 KB) Additional Information: full citation, abstract, references, citings, index

Mobile computing has the potential for managing information globally. Data management issues computing have received some attention in recent times, and the design of adaptive braodcast posed as an important probllem. Such protocols are employed by database servers to decide on bbroadcasts dynamically, in response to client mobility and demand patterns. In this paper we protocols and also propose efficient retrieval s ...

Keywords: adaptive broadcast protocols, client-server computing, energy conservation, mobile

3 VLSI cell placement techniques

K. Shahookar, P. Mazumder

June 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(5.28 MB) Additional Information: full citation, abstract, references, citings, index

VLSI cell placement problem is known to be NP complete. A wide repertoire of heuristic algorith literature for efficiently arranging the logic cells on a VLSI chip. The objective of this paper is to

comprehensive survey of the various cell placement techniques, with emphasis on standard cell placement. Five major algorithms for placement are discussed: simulated annealing, force-direc cut placement, placement by numerical optimization, a ...

Keywords: VLSI, floor planning, force-directed placement, gate array, genetic algorithm, integ layout, min-cut, physical design, placement, simulated annealing, standard cell

4 Frame-sliced partitioned parallel signature files

Fabio Grandi, Paolo Tiberio, Pavel Zezula

June 1992 **Proceedings of the 15th annual international ACM SIGIR conference on Rese development in information retrieval**

Publisher: ACM Press

Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index

The retrieval capabilities of the signature file access method have become very attractive for m applications dealing with both formatted and unformatted data. However, performance is still a when large files are used and fast response required. In this paper, a high performance signatu is proposed, integrating the latest developments both in storage structure and parallel computir combines horizontal and vertical app ...

5 Latency and latch count minimization in wave steered circuits

Amit Singh, Arindam Mukherjee, Malgorzata Marek-Sadowska

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(151.69 KB) Additional Information: full citation, abstract, references, citings, index

Wave Steering is a new design methodology that realizes high throughput circuits by embeddin synthesized structures in silicon. Wave Steered circuits inherently utilize latches in order to gua signal arrival times at the inputs of these synthesized structures and maintain the high through this paper, we show a method of reor-dering signals to achieve minimum circuit latency for Wa and propose an Integer Linear Program ...

6 Computer-assisted microanalysis of parallel programs

Timothy J. Hickey, Jacques Cohen, Hirofumi Hotta, Thierry PetitJean

January 1992 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume

Publisher: ACM Press

Full text available: pdf(3.02 MB) Additional Information: full citation, abstract, references, index terms,

This paper consists of two parts: the first provides the theoretical foundations for analyzing par illustrates how the theory can be applied to estimate the execution time of a class of parallel pr executed on a MIMD computer. The second part describes a program analysis system, based or model, which allows a user to interactively analyze the results of executing (or simulating the e parallel programs. Several examples illustrat ...

Keywords: event graph, execution graph, execution trace, microanalysis, speed up

7 Traffic characterization and SPAM: Measurement based characterization and provisioning

Satish Raghunath, K. K. Ramakrishnan, Shivkumar Kalyanaraman, Chris Chase

October 2004 **Proceedings of the 4th ACM SIGCOMM conference on Internet measurement**

Publisher: ACM Press

Full text available: pdf(533.08 KB) Additional Information: full citation, abstract, references, index terms

Virtual Private Networks provide secure and reliable communication between customer sites. Wi number and size of VPNs, providers need efficient provisioning techniques that adapt to custom

leveraging a good understanding of VPN properties.

In this paper we analyze two important properties of VPNs that impact provisioning - (a) structu endpoint (CE) interactions and (b) temporal characteristics of CE-CE traffic. We deduce these pı compu ...

Keywords: VPN, matrix estimation, provisioning, traffic, traffic engineering

8 Architecture analysis and automation: An FPGA architecture with enhanced datapath funct

Katarzyna Leijten-Nowak, Jef L. van Meerbergen

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on l programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(188.86 KB) Additional Information: full citation, abstract, references, index terms

Although FPGAs are a cost-efficient alternative for both ASICs and general purpose processors, designs which are more than an order of magnitude more costly and slower than their equivaler dedicated logic. This efficiency gap makes FPGAs less suitable for high-volume cost-sensitive ap embedded systems).We show that the intrinsic cost of traditional general-purpose FPGAs can be designed to target an application domain or a ...

Keywords: DSP, FPGAs, adder inverting property, application-domain tuning, logic block archit

9 A pipelined memory architecture for high throughput network processors

Timothy Sherwood, George Varghese, Brad Calder

May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual symposium on Computer architecture ISCA '03**, Volume 31 Issue 2

Publisher: ACM Press

Full text available: pdf(213.66 KB) Additional Information: full citation, abstract, references, citings

Designing ASICs for each new generation of backbone routers is a time intensive and fiscally dr this paper we focus on the design of a programmable architecture for backbone routers, based of wide irregular memory words, that can provide a feasible design alternative to custom ASICs pipelined memory design that emphasizes worst-case throughput over latency, and co-explore a tradeoffs with the design of several important network algo ...

10 Enriching the lambda calculus with contexts: toward a theory of incremental program consi

Shinn-Der Lee, Daniel P. Friedman

June 1996 **ACM SIGPLAN Notices , Proceedings of the first ACM SIGPLAN international c Functional programming ICFP '96**, Volume 31 Issue 6

Publisher: ACM Press

Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, citings, index

A context in the λ-calculus is a term with some holes. Hole filling differs from β-su name capture is intended. This seemingly simple feature transcends static scope and lies at the and object-oriented programming. Still, the name capture feature of hole filling is at odds with l substitution. In this paper we conservatively extend the λ-calculus to incorporate the n without jeopardizing the & ...

11 Detecting shifts in news stories for paragraph extraction

Fumiyo Fukumoto, Yoshimi Suzuki

August 2002 **Proceedings of the 19th international conference on Computational linguistic**

Publisher: Association for Computational Linguistics

Full text available: pdf(238.41 KB) Additional Information: full citation, abstract, references

For multi-document summarization where documents are collected over an extended period of t a document changes over time. This paper focuses on subject shift and presents a method for e paragraphs from documents that discuss the same *event.* Our extraction method uses the resul which starts from a few sample documents and finds all subsequent documents that discuss the method was tested on the TDT1 corpus, an ...

12 Multiresolution curves

Adam Finkelstein, David H. Salesin

July 1994 **Proceedings of the 21st annual conference on Computer graphics and interac**

Publisher: ACM Press

Full text available: pdf(906.94 KB) ps (908.68 KB) Additional Information: full citation, abstract, references, citings, index

We describe a multiresolution curve representation, based on wavelets, that conveniently suppc operations: smoothing a curve; editing the overall form of a curve while preserving its details; a curve within any given error tolerance for scan conversion. We present methods to support con smoothing as well as direct manipulation of an arbitrary portion of the curve; the control points discrete nature of the underlying hierarch ...

Keywords: curve compression, curve editing, curve fitting, curve smoothing, direct manipulati wavelets

13 Architectural support for reduced register saving/restoring in single-window register files

Miquel Huguet, Tomás Lang

February 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 1

Publisher: ACM Press

Full text available: pdf(2.28 MB) Additional Information: full citation, abstract, references, citings, index

The use of registers in a processor reduces the data and instruction memory traffic. Since this r significant factor in the improvement of the program execution time, recent VLSI processors ha of registers which can be used efficiently because of the advances in compiler technology. Howe have to be saved/restored across function calls, the corresponding register saving and restoring traffic can almost eliminate the overall reduc ...

14 Research sessions: security and privacy: Secure XML querying with security views

Wenfei Fan, Chee-Yong Chan, Minos Garofalakis

June 2004 **Proceedings of the 2004 ACM SIGMOD international conference on Managem**

Publisher: ACM Press

Full text available: pdf(229.47 KB) Additional Information: full citation, abstract, references

The prevalent use of XML highlights the need for a generic, flexible access-control mechanism f that supports efficient and secure query access, without revealing sensitive information unauth paper introduces a novel paradigm for specifying XML security constraints and investigates the constraints during XML query evaluation. Our approach is based on the novel concept of *securit* provide for each user group (a) an XML view ...

15 Reverse engineering: Recovering software requirements from system-user interaction trac

Mohammad El-Ramly, Eleni Stroulia, Paul Sorenson

July 2002 **Proceedings of the 14th international conference on Software engineering ar engineering SEKE '02**

Publisher: ACM Press

Full text available: pdf(112.21 KB) Additional Information: full citation, abstract, references, citings

As software systems age, the requirements that motivated their original development get lost. I documentation is unavailable or obsolete. Recapturing these requirements is critical for softwar

activities. In our CelLEST process we adopt a data-mining approach to this problem and attemp patterns of frequent similar episodes in the sequential run-time traces of the legacy user-interfa patterns constitute operational models of the application ...

16 Fortran 8X draft

Loren P. Meissner

December 1989 **ACM SIGPLAN Fortran Forum**, Volume 8 Issue 4

Publisher: ACM Press

Full text available: pdf(21.36 MB) Additional Information: full citation, abstract, index terms

Standard Programming Language Fortran. This standard specifies the form and establishes of programs expressed in the Fortran language. It consists of the specification of the language f are specified in this standard. The previous standard, commonly known as "FORTRAN 77", is en within this standard, known as "Fortran 8x". Therefore, any standard-conforming FORTRAN 77 p conforming under this standard. New features can b ...

17 An overview of deterministic functional RAM chip testing

A. J. van de Goor, C. A. Verruijt

March 1990 **ACM Computing Surveys (CSUR)**, Volume 22 Issue 1

Publisher: ACM Press

Full text available: pdf(2.49 MB) Additional Information: full citation, abstract, references, citings, index

This paper presents an overview of deterministic functional RAM chip testing. Instead of the tra approach toward developing memory test algorithms, a hierarchy of functional faults and tests i is shown to cover all likely functional memory faults. This is done by presenting a novel way of faults. All (possible) fault combinations are discussed. Requirements are put forward under whic combination can be detected. Finally, ...

18 The feudal priority algorithm on hidden-surface removal

Han-Ming Chen, Wen-Teng Wang

August 1996 **Proceedings of the 23rd annual conference on Computer graphics and interac**

Publisher: ACM Press

Full text available: pdf(180.31 KB) Additional Information: full citation, references, citings, index terms

Keywords: the binary space partitioning tree algorithm

19 Resolving uncertainties during trace analysis

Alexander Egyed

October 2004 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 12th ACM SI(international symposium on Foundations of software engineering SIGSOFT '(** 29 Issue 6

Publisher: ACM Press

Full text available: pdf(481.02 KB) Additional Information: full citation, abstract, references, index terms

Software models provide independent perspectives onto software systems. Ideally, all models s model element to describe the same part of a system. Practically, models elements are not shai syntactic and semantic differences among modeling notations. Trace dependencies explicitly ma commonalities among the distinct model elements.

Generating and maintaining trace dependencies is difficult, costly, and highly error-prone. Auto analysis ...

20 A framework for the integration of partial evaluation and abstract interpretation of logic pro(

Michael Leuschel
May 2004 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume
Publisher: ACM Press
Full text available: pdf(319.71 KB) Additional Information: full citation, abstract, references, index terms

Recently the relationship between abstract interpretation and program specialization has receiv
and the need has been identified to extend program specialization techniques so as to make us
abstract domains and operators. This article clarifies this relationship in the context of logic pro
expressing program specialization in terms of abstract interpretation. Based on this, a novel spe
framework, along with generic correctness results ...

Keywords: Partial deduction, abstract interpretation, flow analysis, logic programming, partial
transformation

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